

Fig. 2a PRIOR ART

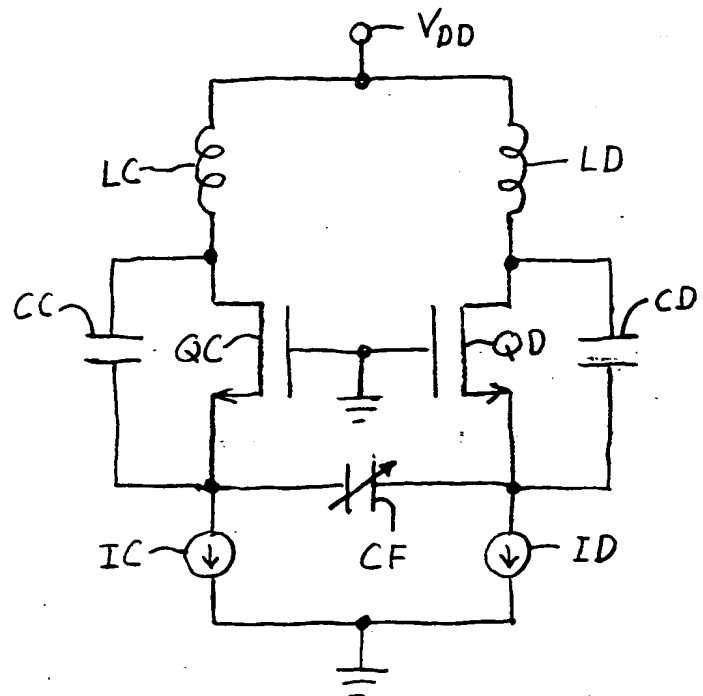


Fig. 2b PRIOR ART

Fig. 3  
PRIOR ART

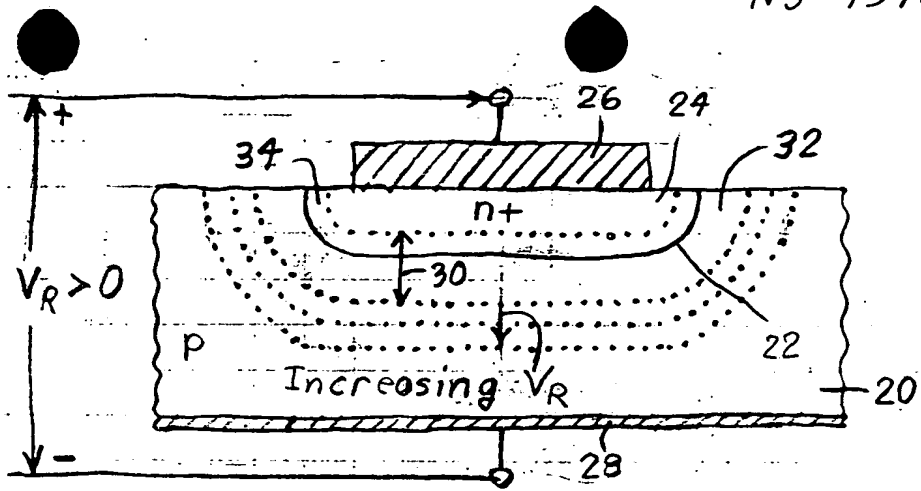


Fig. 4  
PRIOR ART

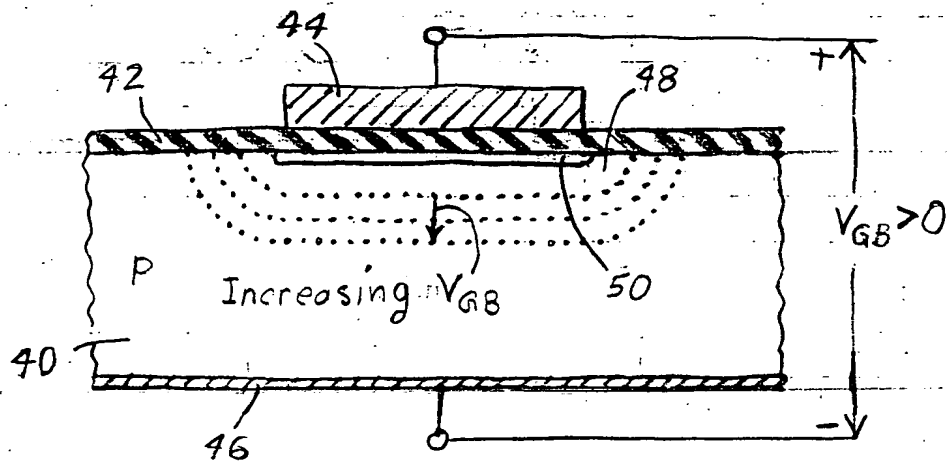
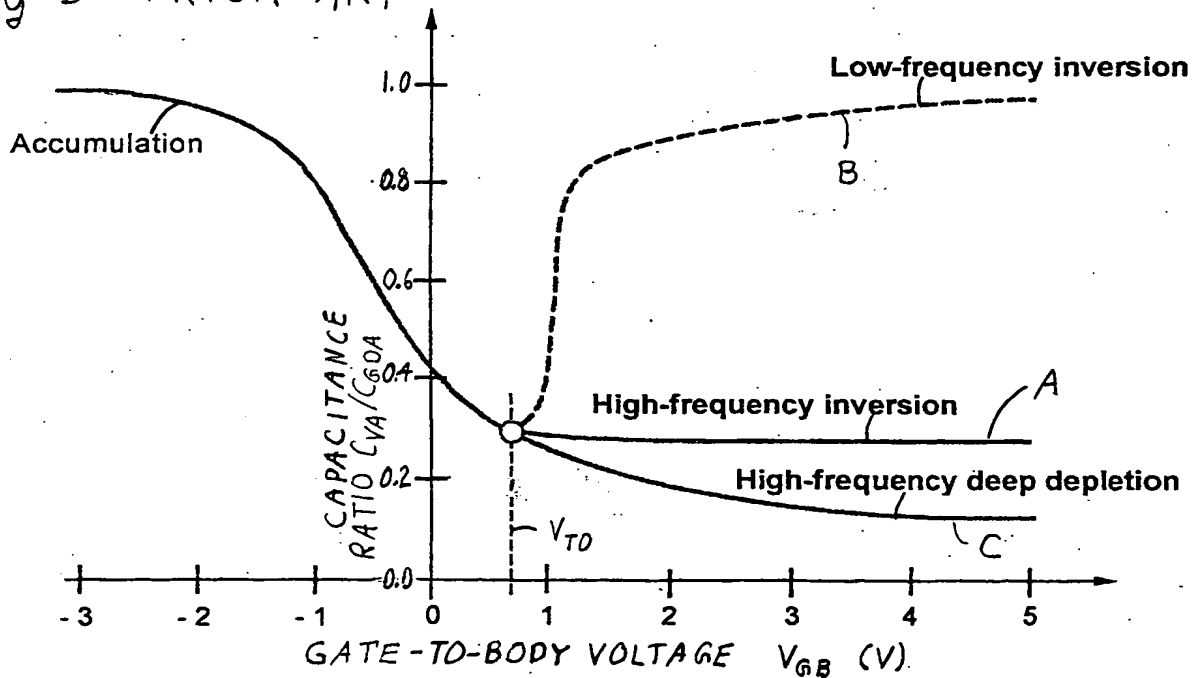


Fig 5 PRIOR ART



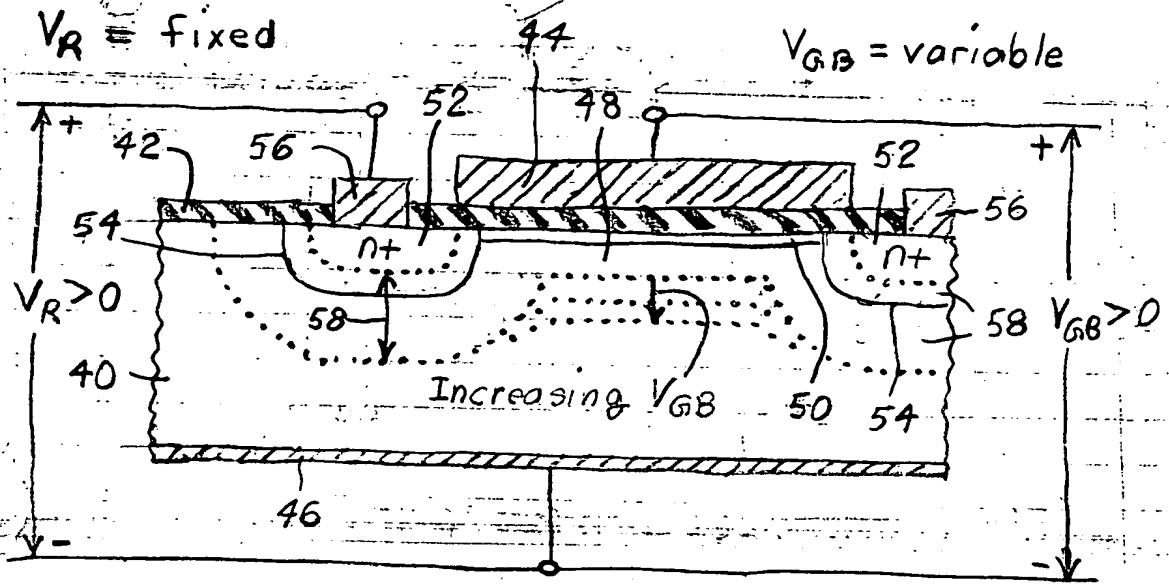


Fig. 6 PRIOR ART

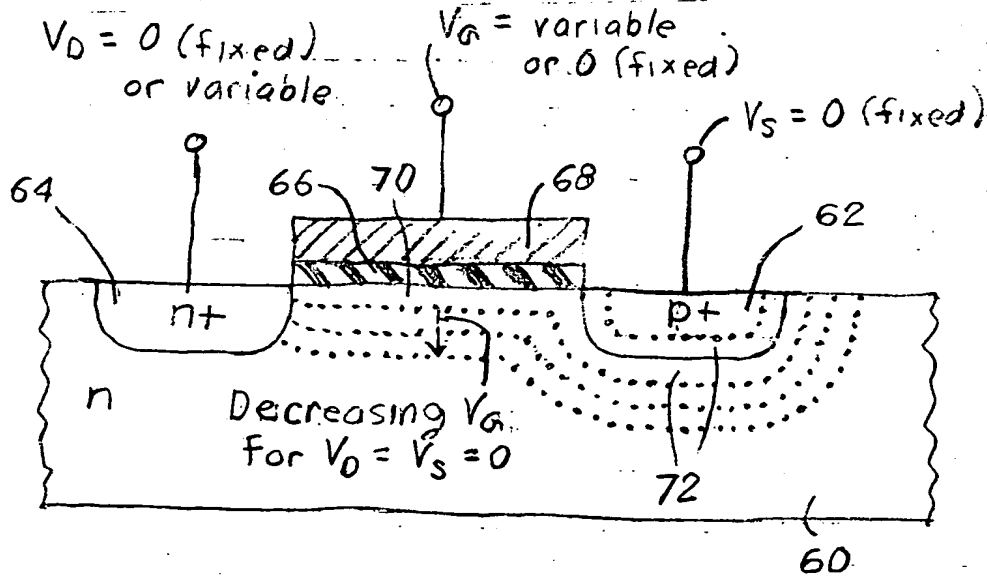


Fig. 7 PRIOR ART

[illegible]

Diagram illustrating a cross-sectional view of a semiconductor device structure, likely a MOSFET, showing various layers and regions. The structure includes a substrate 100, a gate stack 110, and a channel region 106. The gate stack 110 consists of a gate oxide 114 and a gate 112. The channel region 106 is formed in the substrate 100. The diagram also shows a source/drain region 104, a gate oxide 116, and a gate oxide 118. The diagram is labeled with various parameters:  $V_p$ ,  $V_g$ ,  $V_R > 0$ ,  $V_{GB} > 0$ ,  $V_R \geq V_x > 0$ , and Increasing  $V_R$ .

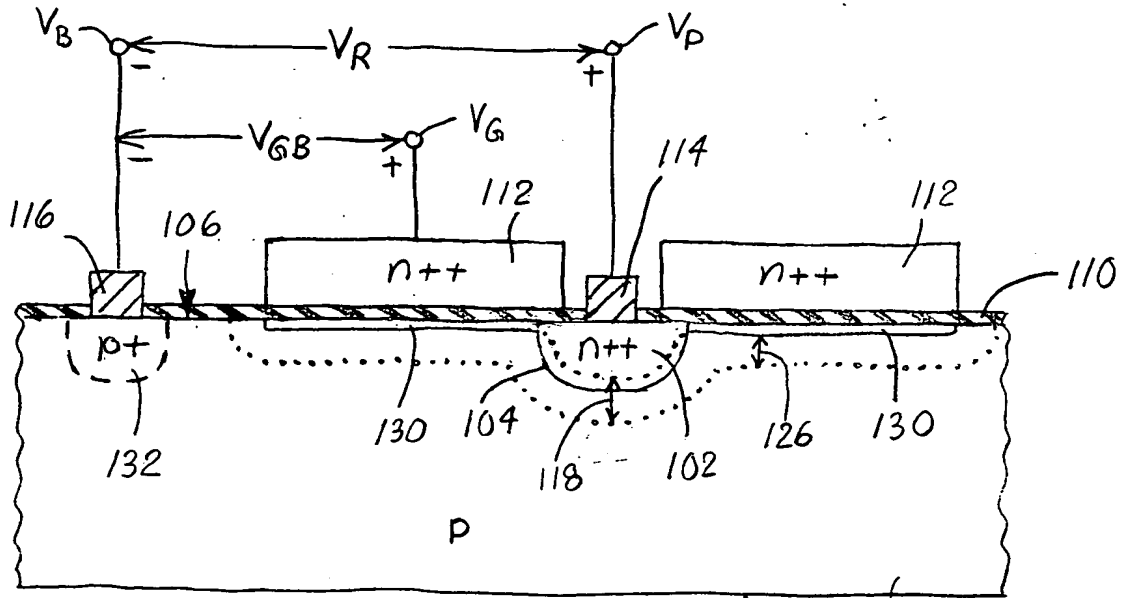


Fig. 9a

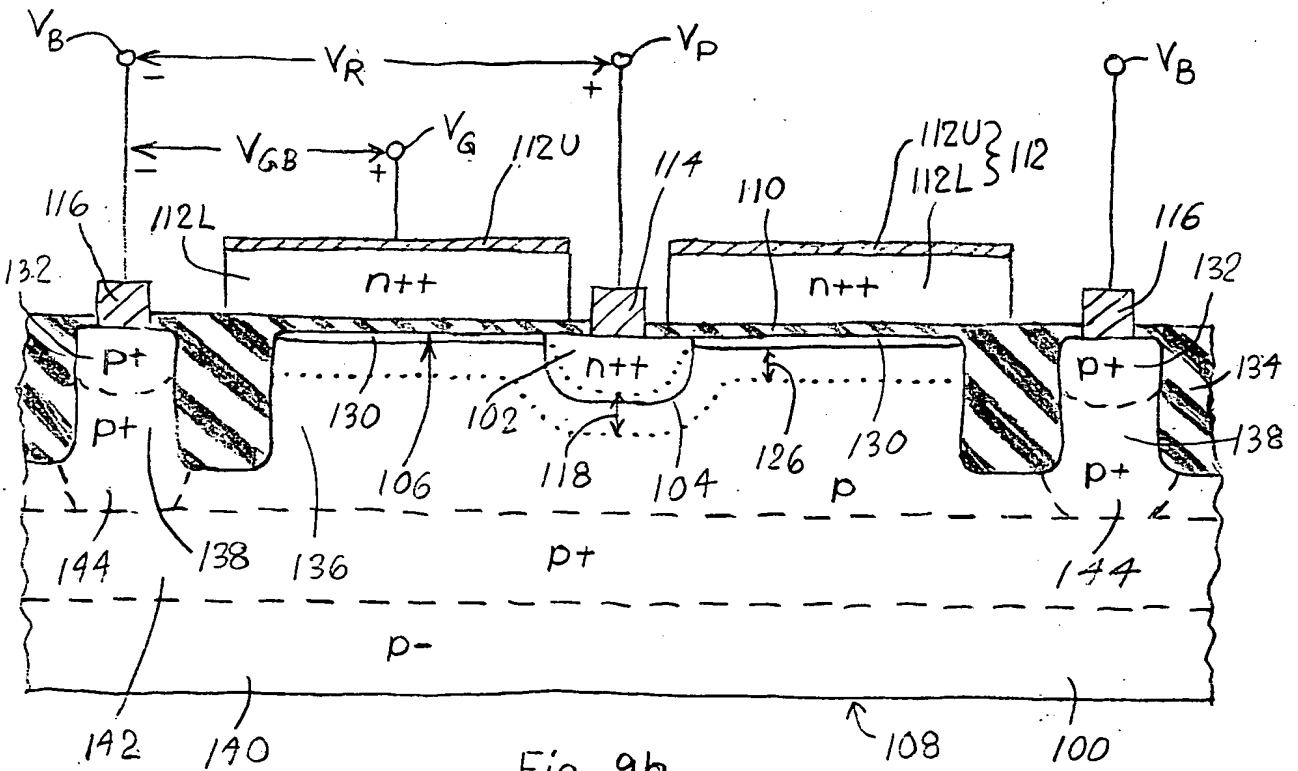
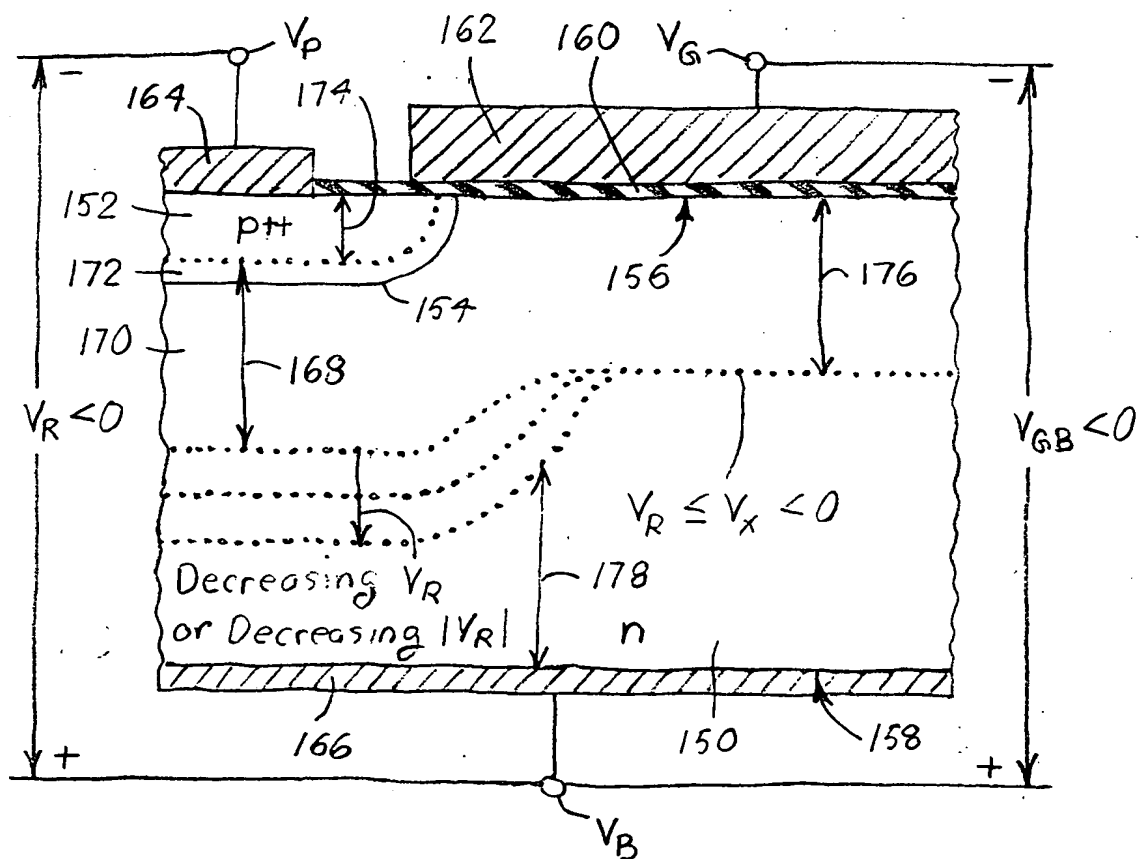
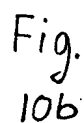


Fig. 9b

100T/0"6506060



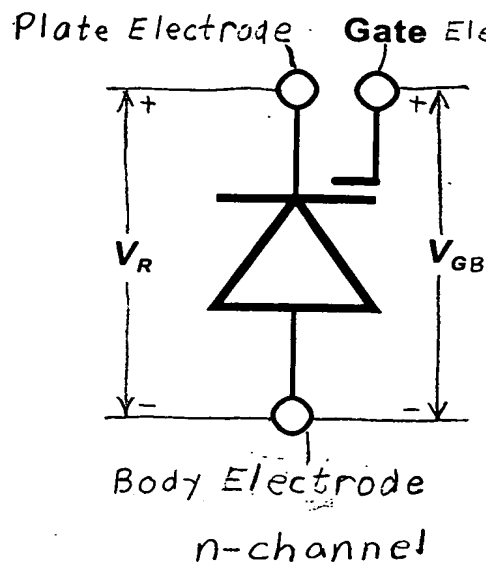


Fig. 11a

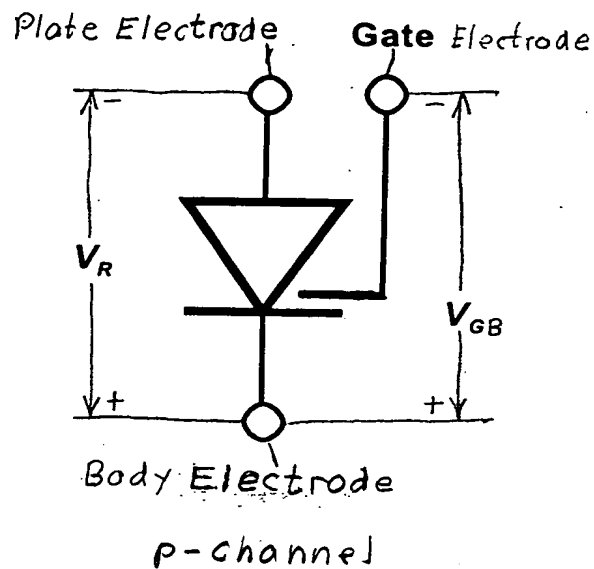


Fig. 11b

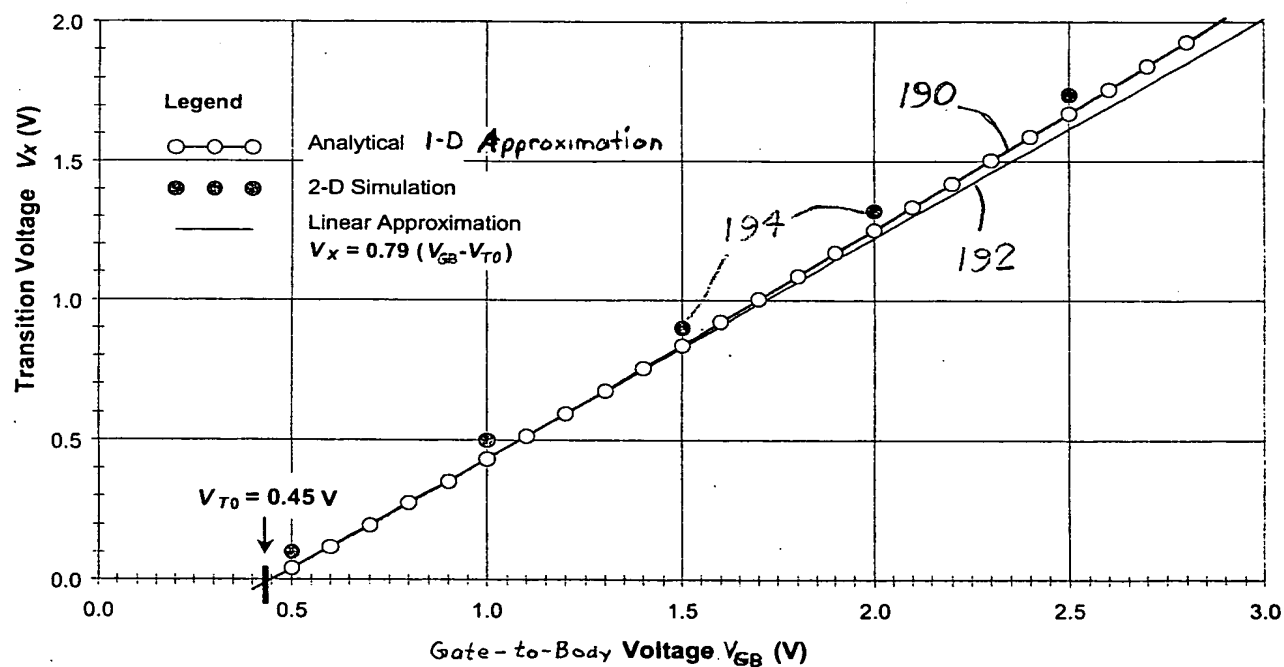


Fig. 12

FOOT/0" 650E0660

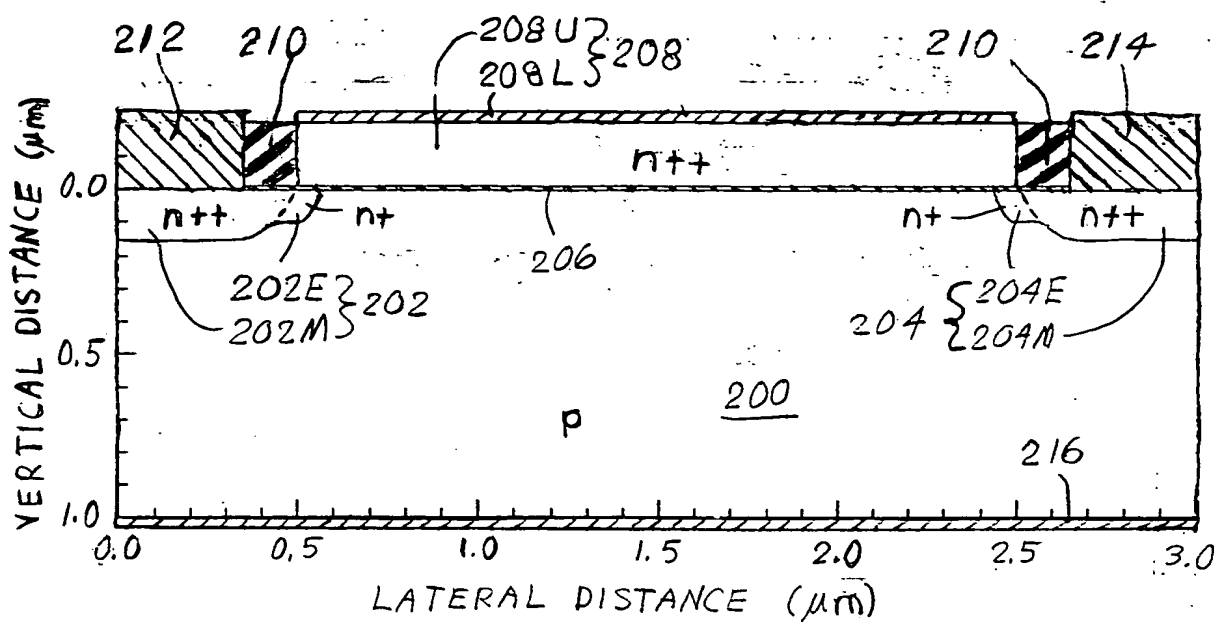


Fig. 13

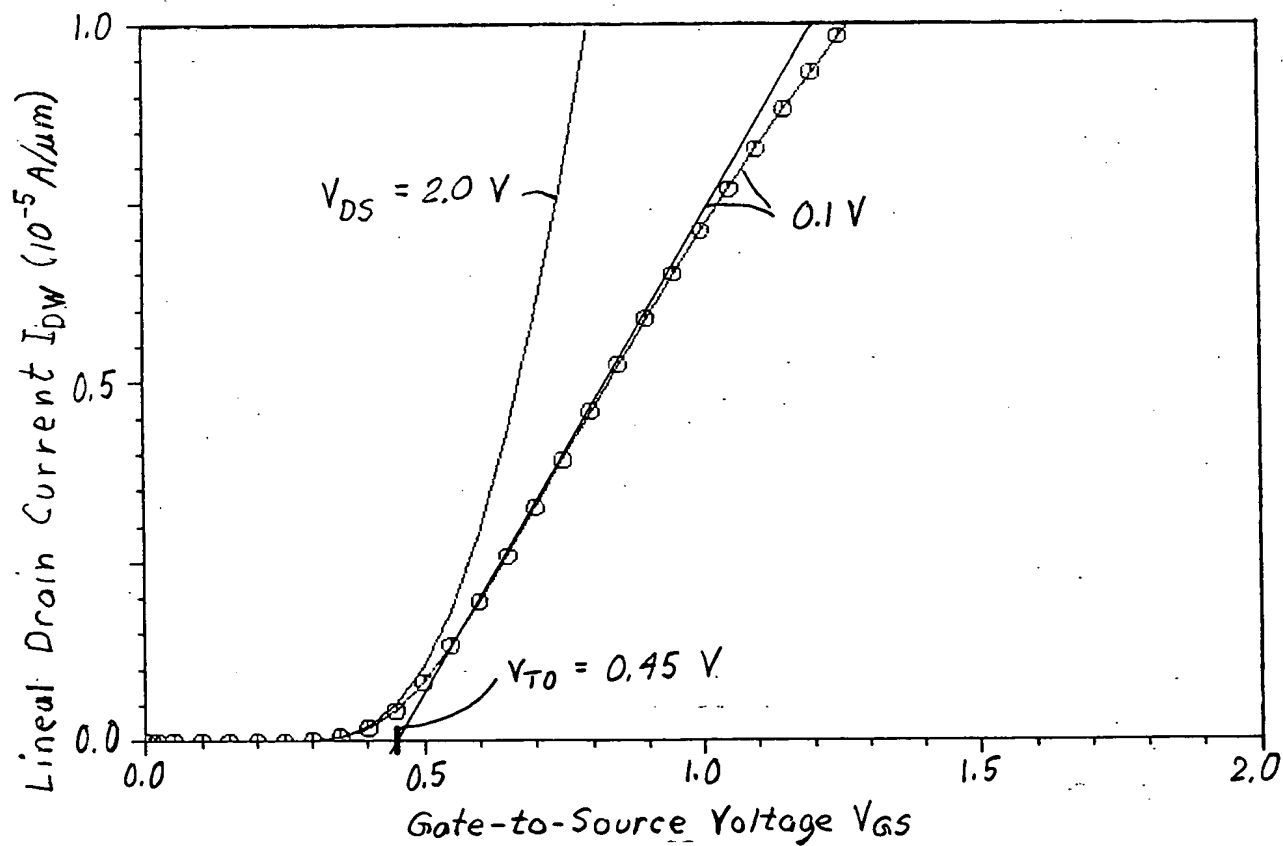


Fig. 14



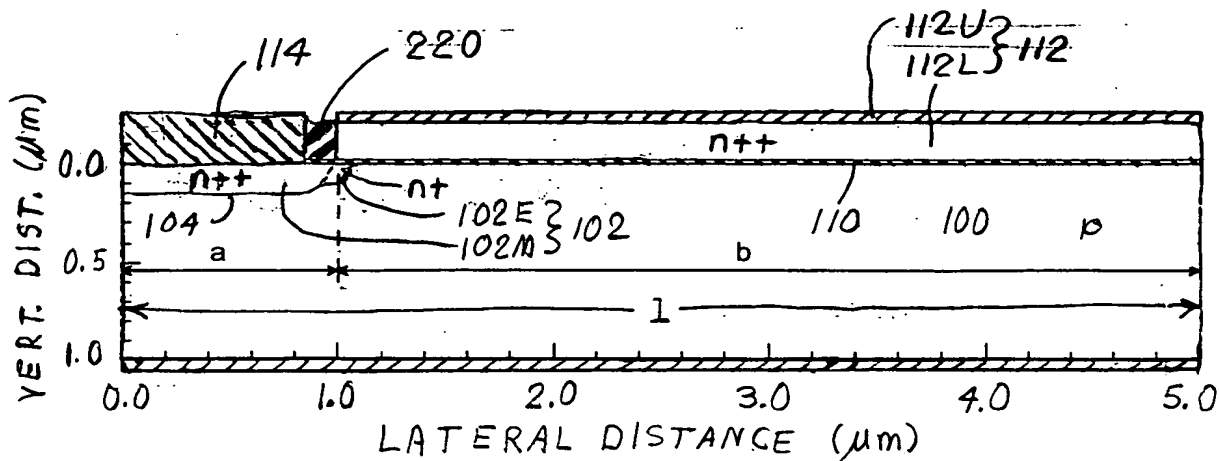


Fig. 15

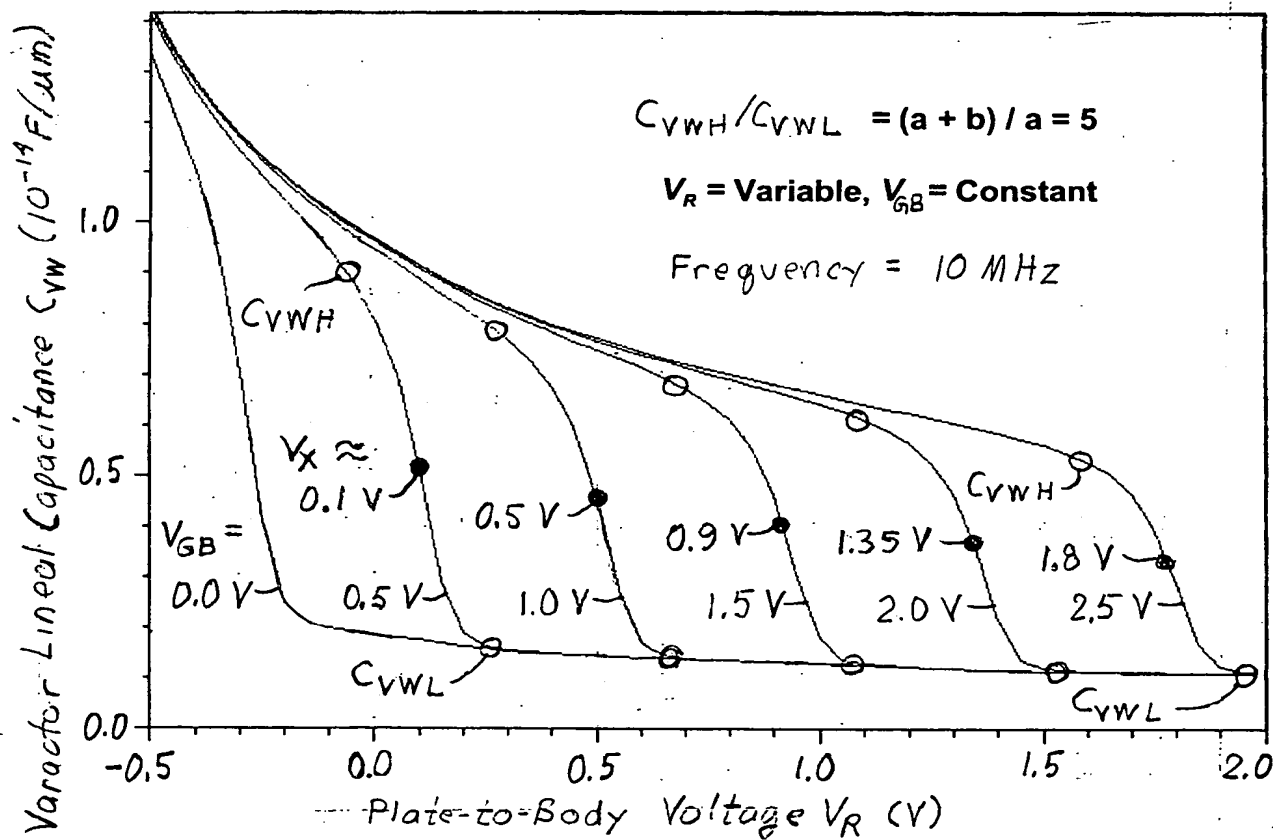


Fig. 16

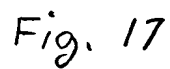
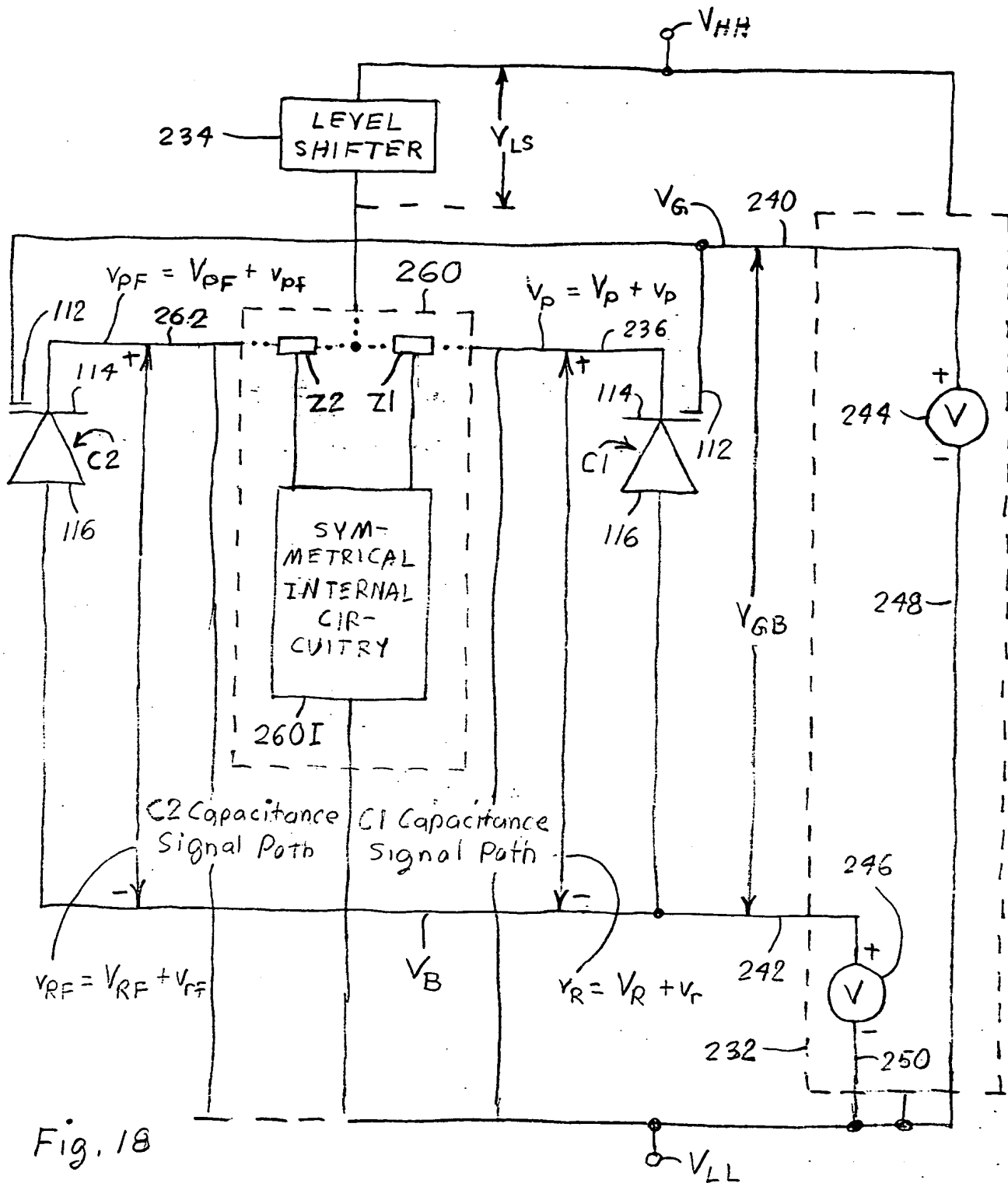


Fig. 17

0650E650 071001



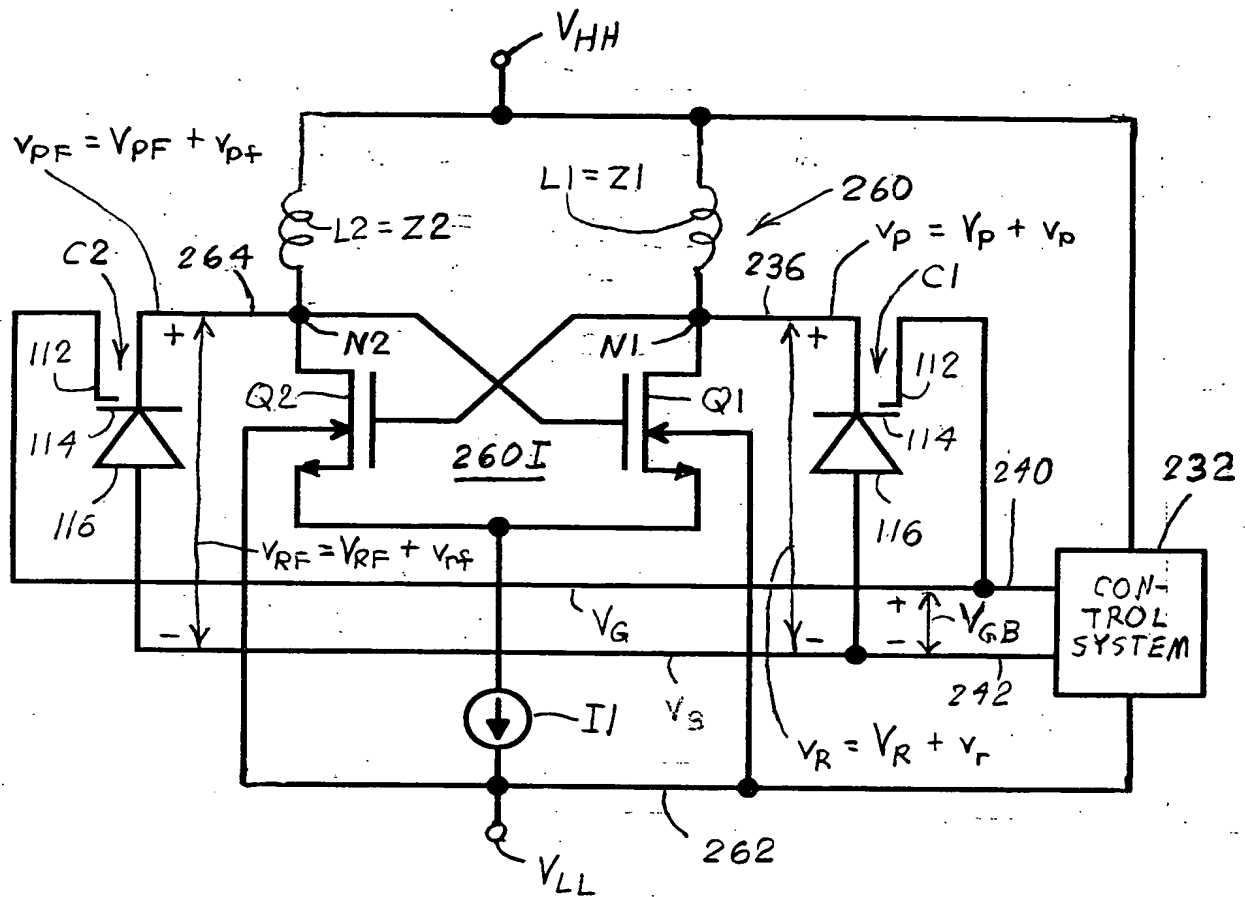
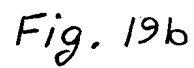


Fig. 19a



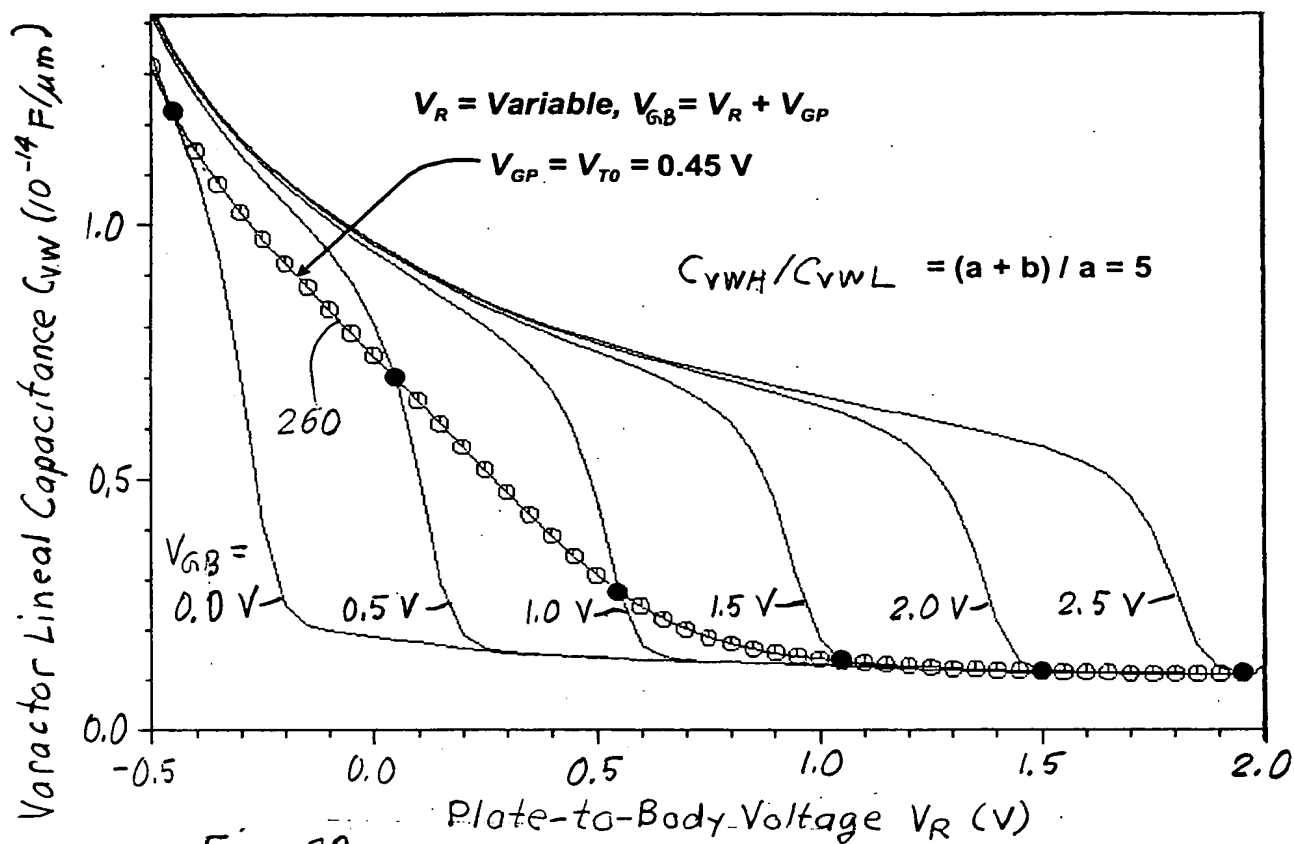


Fig. 20a

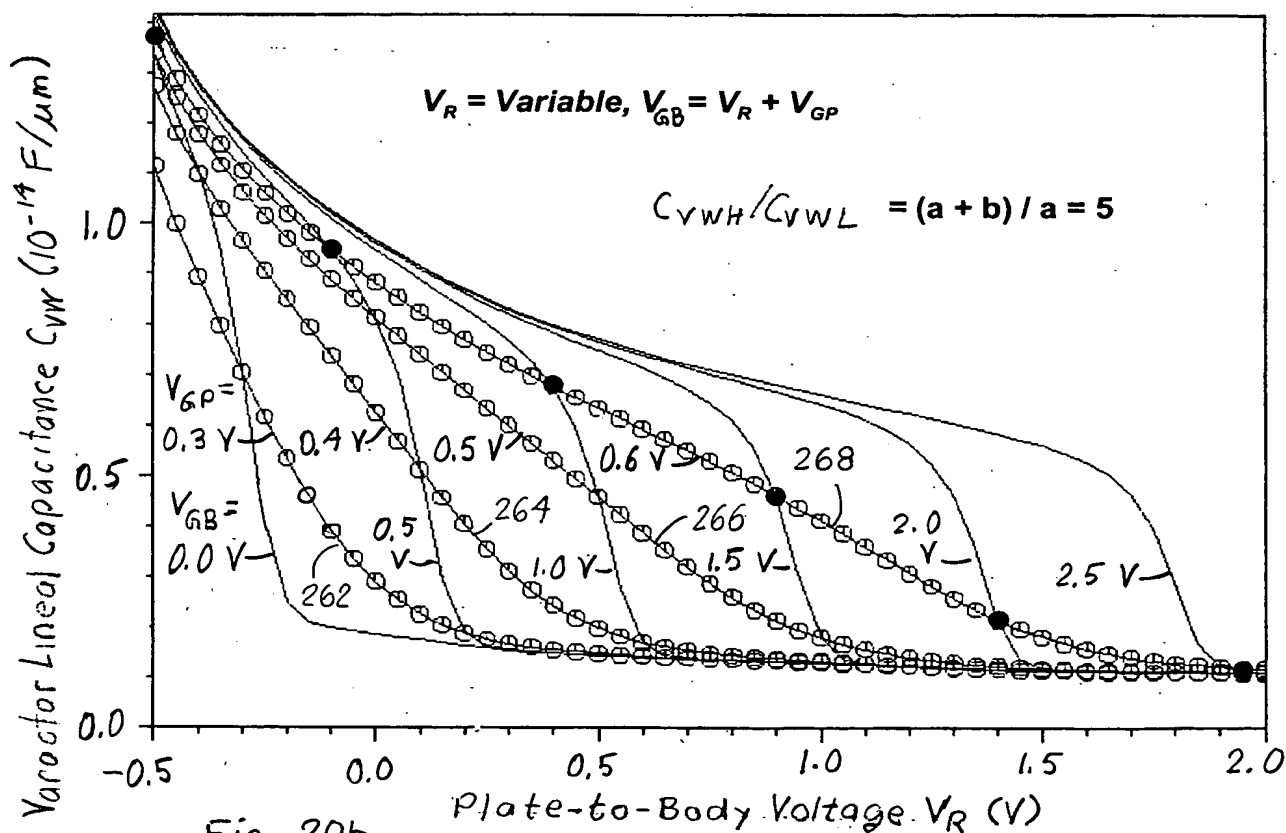


Fig. 20b

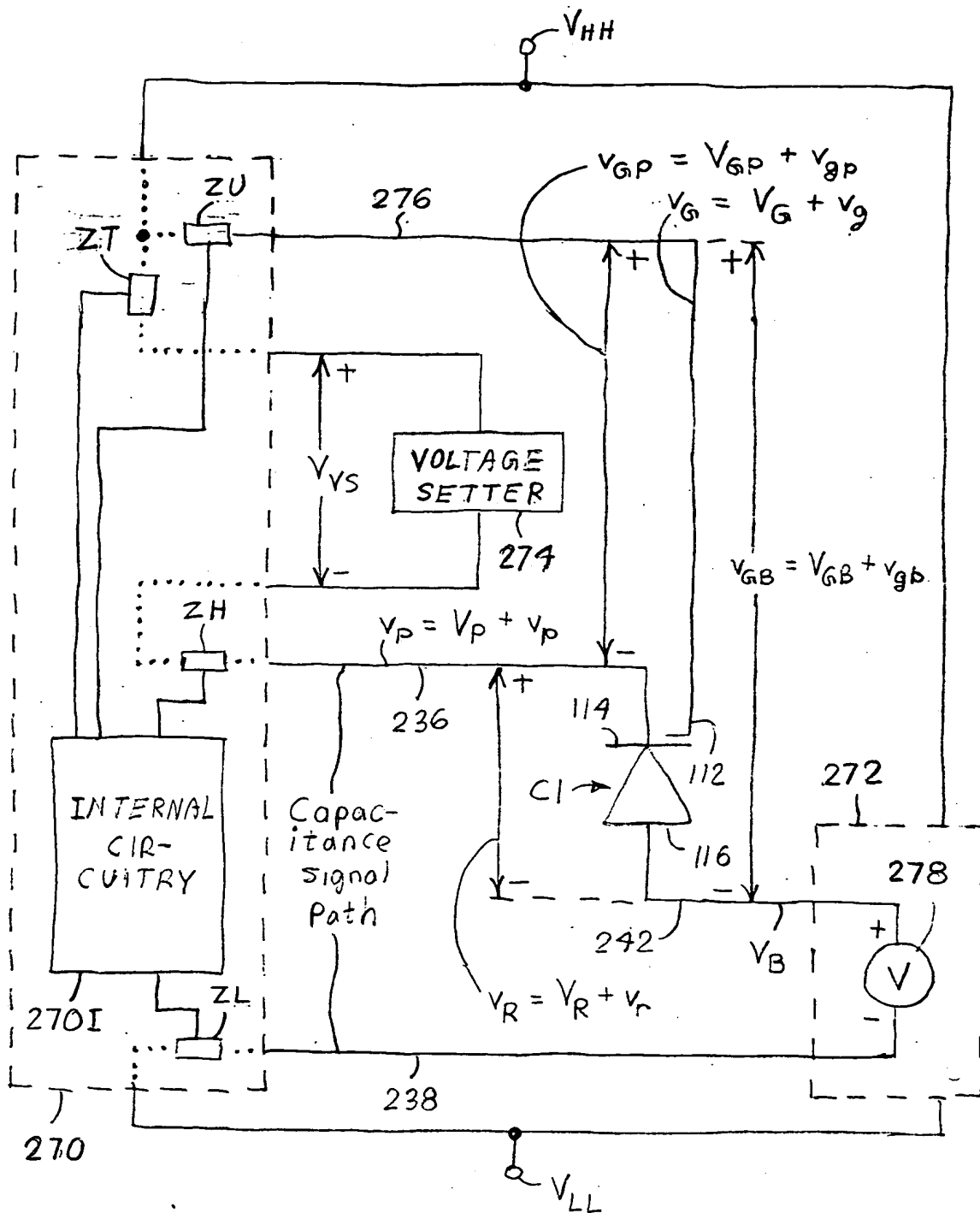
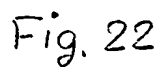


Fig. 21





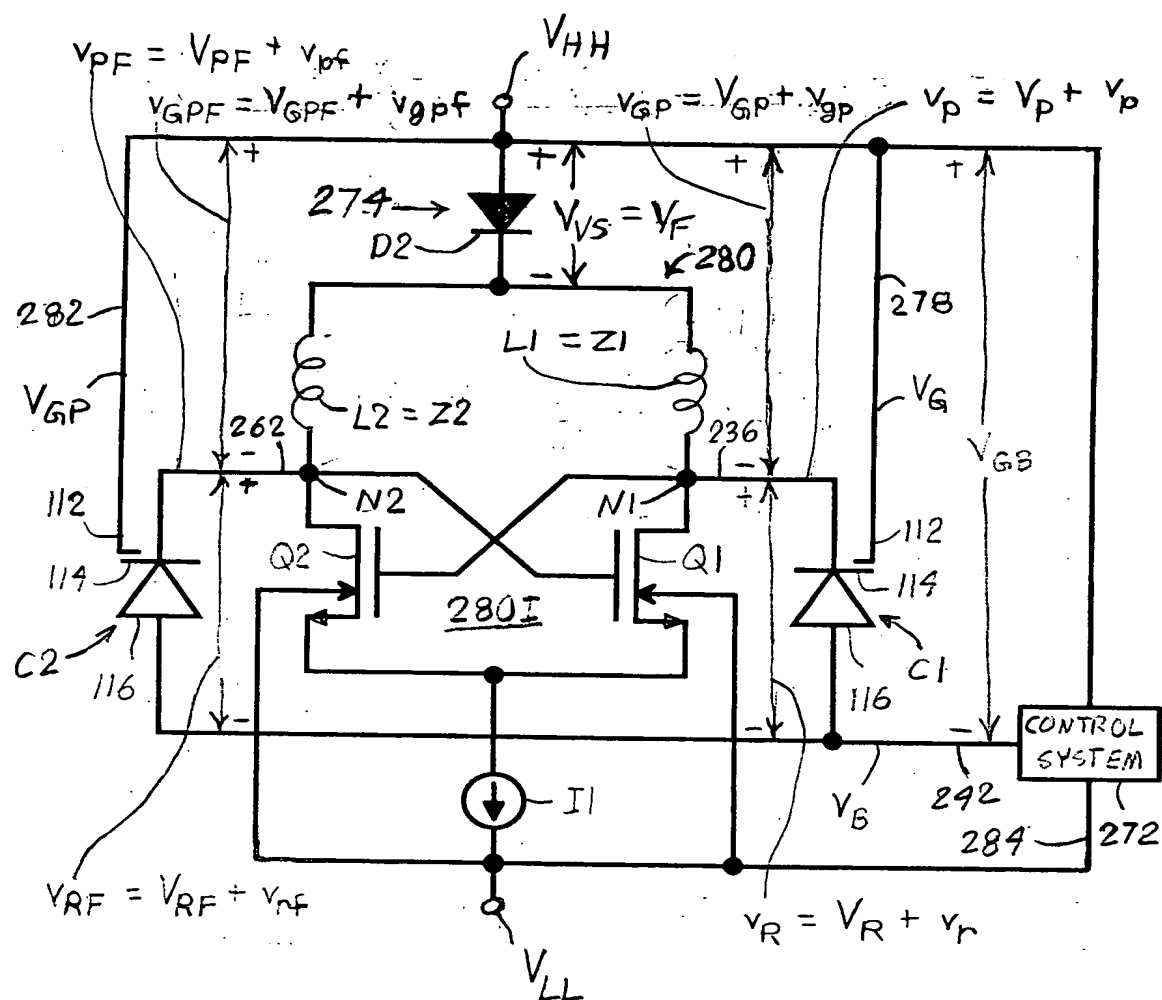


Fig. 23a

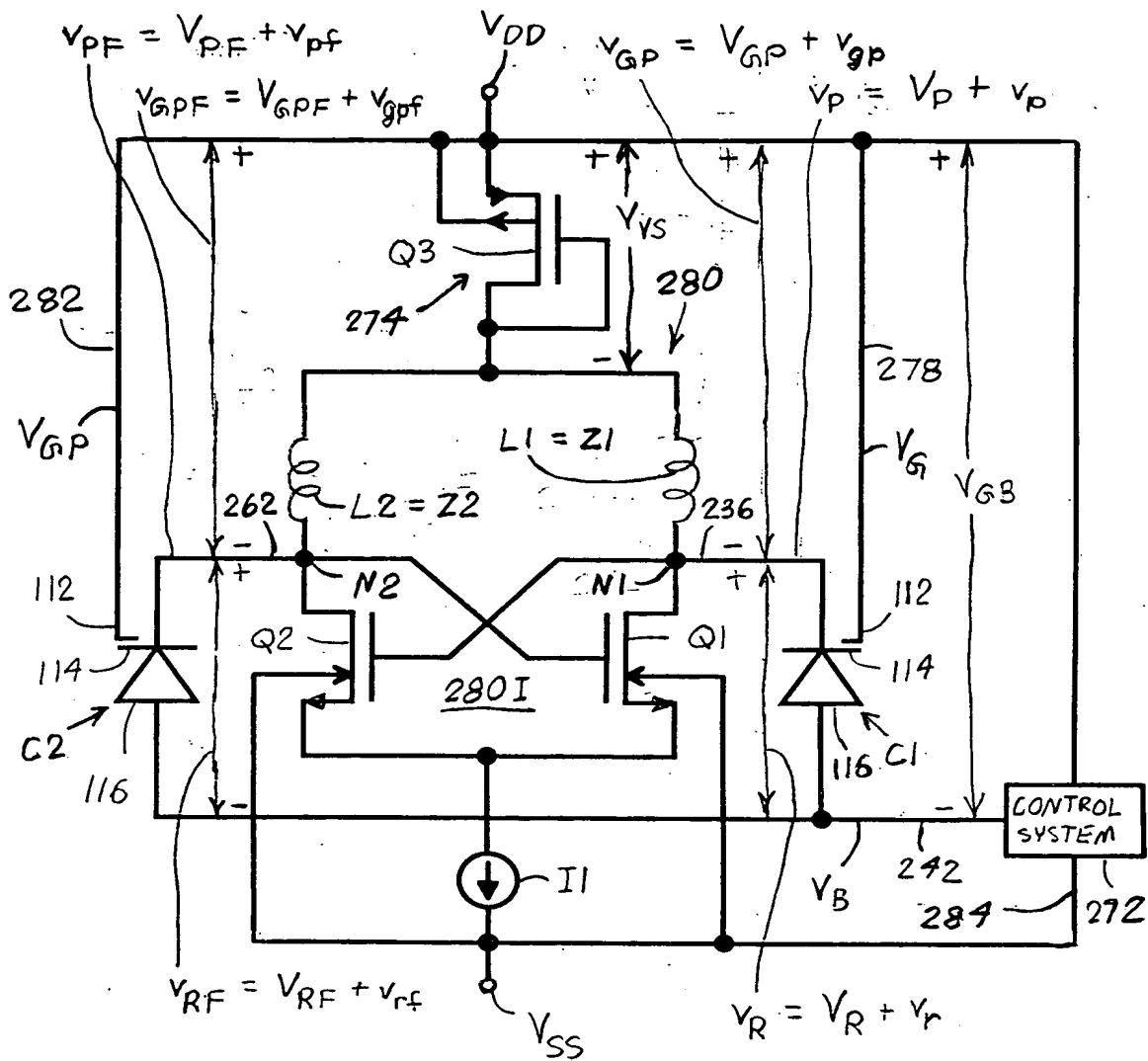


Fig. 23b

09903059-01001

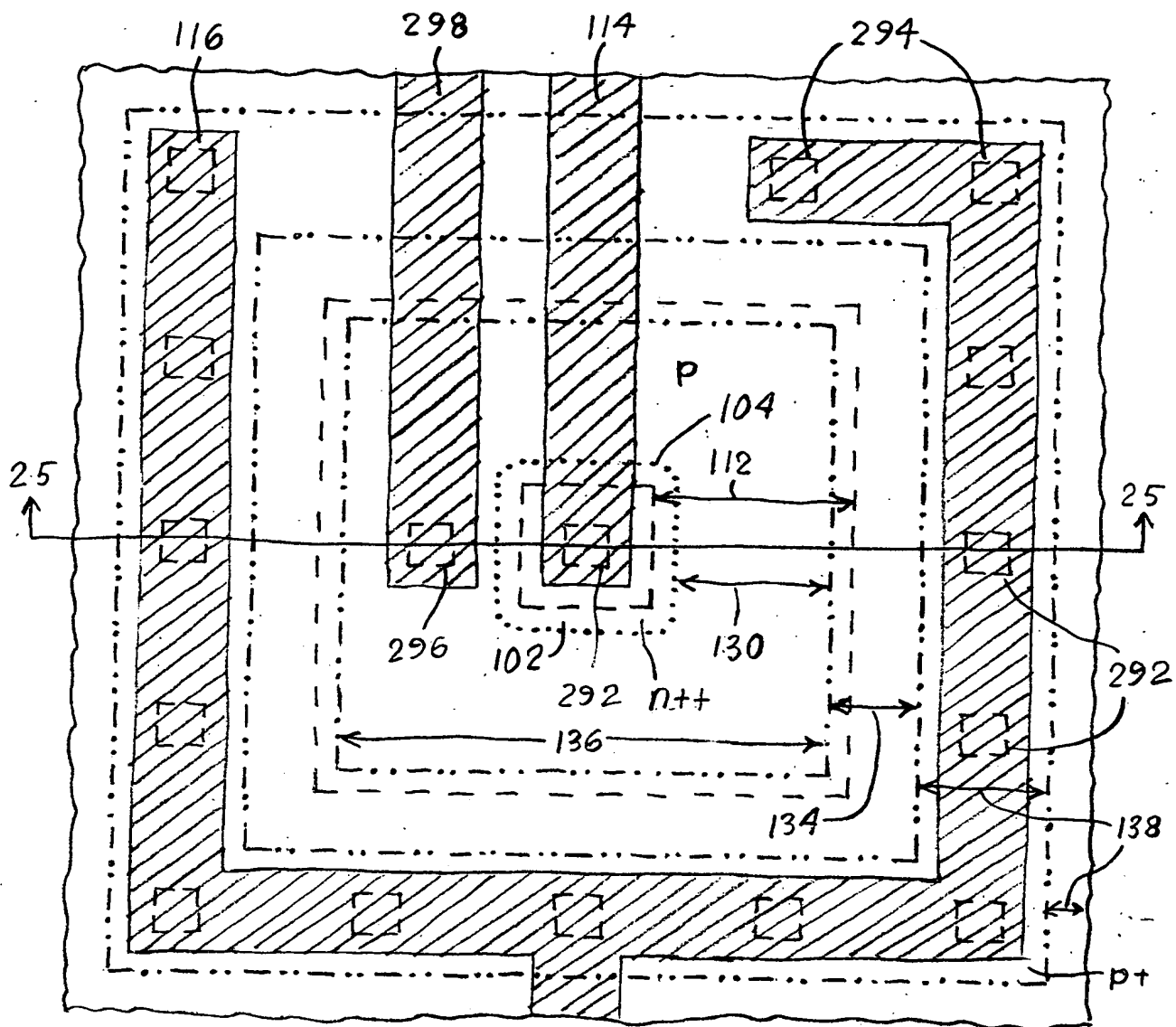


Fig. 24

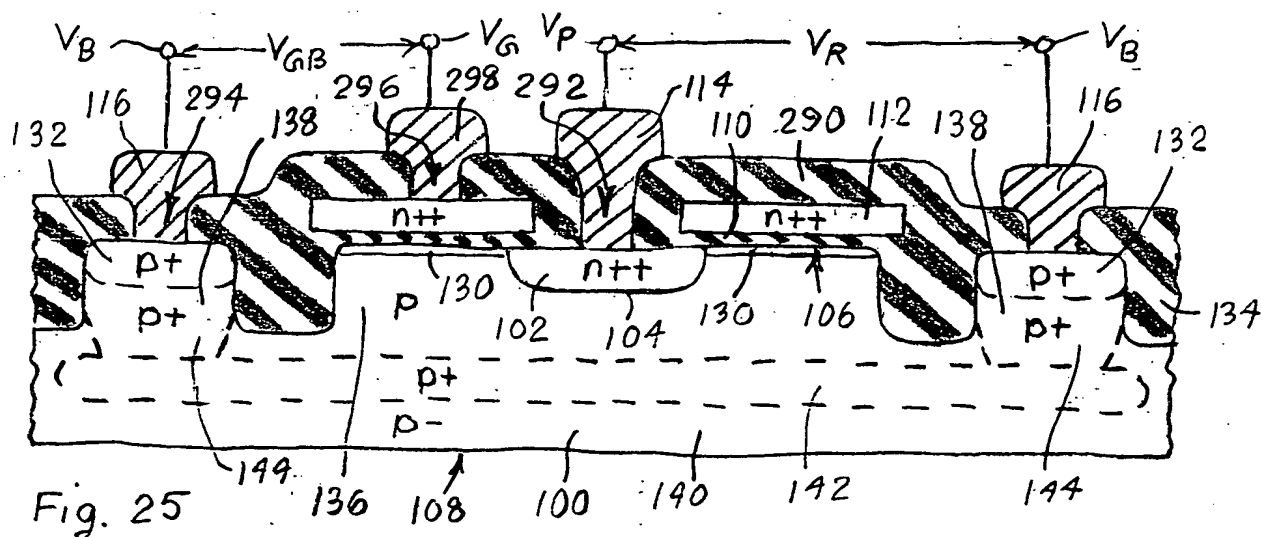


Fig. 25

